REMARKS

In the Office Action, Claims 1-20 were examined and stand rejected. In response to the Office Action, Claims 1, 2, 8 and 17 are amended, no claims are cancelled and no claims are added. Applicant respectfully requests reconsideration of pending Claims 1-20 in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. §112

Claims 1, 2, 8 and 17 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement.

Regarding Claim 1, Claim 1 is amended to recite:

> a command register coupled to the plurality of states to store test data for use with the plurality of states.

Support for such amendment is provided at pg. 7, ¶ 20 of Applicant's specification, wherein it is stated:

> In one embodiment, the state machine allows the full RAM width of unique write data to be written at one time or one 16-bit pattern to be written to the entire width, as opposed to each bit being written individually. (pg. 7, ¶ 20.)

Applicant respectfully submits that the cited passage provides support for Applicant's amendment to Claim 1 and provides sufficient description to enable one skilled in the art to make and/or use the invention. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the 35 U.S.C. §112, first paragraph, rejection of Claim 1.

Regarding Claims 2, 8 and 17, Claims 2, 8 and 17 have been amended to recite the following claim feature:

> . . . wherein the plurality of states consists of only four states to ensure that no more than four states are used by the BIST state machine for a test.

As indicated in Applicant's specification:

> The BIST state machine is a four state machine that accommodates a large group of test suites by programming each state to have the capability of performing four operations. (pg. 6, ¶ 17.)

Accordingly, based on the cited passage above, Applicant respectfully submits that the cited passage provides support for Applicant's amendment to Claims 2, 8 and 17 and is sufficient to enable one skilled in the art to make and use the invention. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the 35 U.S.C. §112, first paragraph, rejection of Claims 2, 8 and 17.

Claims 2, 8 and 17 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

As indicated above with reference to Claims 2, 8 and 17, Claims 2, 8 and 17 have been amended such that the claims now recite:

> . . . no more than four states are used by the BIST state machine.

Accordingly, Applicant respectfully submits that Claims 2, 8 and 17, as amended, now particularly point out and distinctly claim the subject matter, which Applicant regards as the invention. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the 35 U.S.C. §112, second paragraph, rejection of Claims 2, 8 and 17.

II. Claims Rejected Under 35 U.S.C. §103

The Examiner rejects Claims 1, 7 and 16 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,760,865 issued to Ledford et al. ("Ledford") in view of U.S. Patent No. 6,415,403 issued to Huang et al. ("Huang"). Applicant respectfully traverses this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142)

According to the Examiner:

> Each state of state machine 51 controls the operations of state machine 70 (nested states), and therefore all functions of 70 are executed in any state of 51. (Example: col. 5, lines 54-63.) (*See*, pg. 4, ¶ 1 of Office Action mailed August 26, 2004.)

Applicant respectfully disagrees with the Examiner's contention. Specifically, as indicated by Ledford:

Initialization of predetermined values into timer 72, data generator and comparator 74 and address generator 76 is required due to the fact that differing memory arrays may be used which have differing operating characteristics. (col. 5, lines 11-15.) (Emphasis added.)

As further described within Ledford:

State machine 51 controls the initialization mode. Additionally, state machine 51 controls the command sequencing to complete the BIST operation. (col. 4, lines 17-19.) (Emphasis added.)

As further described by Ledford:

State machine 51 sends a command to state machine 70 to start the initialization routine . . . the programming of data is under control of a test algorithm being executed by state machine 70. State machine 51 launches state machine 70 with a single command to begin execution of a predetermined test algorithm. (col. 5, lines 39-48.) (Emphasis added.)

Based on the cited passages above, Applicant respectfully submits that the state machine 51 operates according to an initialization state and a test execution state. Likewise, state machine 70 includes an initialization state and a test execution state. In addition, state machine 70 includes an initialization state, as well as the test state. However, Applicant respectfully submits that Ledford teaches away from state machine 51 during its initialization state to issue a command to launch state machine 70 to begin execution of a predetermined test algorithm.

Applicant's argument is based on the previously-cited passage indicating that initialization of predetermined values is required due to the fact that differing memory arrays may be used, which have differing operating characteristics. (*See*, col. 5, lines 11-15.) Accordingly, based on the cited passages above, Applicant respectfully submits that Ledford teaches away from all functions of state machine 70 being executed in any state machine 51, as contended by the Examiner.

As correctly pointed-out by the Examiner, Ledford fails to teach that each state is capable of performing a null operation, a write operation, a read operation and a read/write operation, by name. But in an analogous art, Huang discloses the operations executed by name in col. 6, lines 14-58 and FIG. 4. (*See*, pg. 4, ¶ 1 of Office Action mailed August 26, 2004.) As described by Huang:

In FIG. 4 is shown the state diagram of the sequence controller finite state machine for march and refresh tests. Timing sequence generation modules, as shown as circles in FIG. 4, are implemented for single read/write command 63 and page mode (Pg m) read/write command 64 for march tests defined in the controller 11. (col. 6, lines 14-19.) (Emphasis added.)

However, as recited by Claim 1:

. . . each state capable of performing a null operation, a write operation, a read operation, and a read/write operation. (Emphasis added.)

Conversely, as illustrated in FIG. 4 of Huang, only reset state 61 is capable of performing a null operation, a write operation, a read operation, and a read/write operation, as recited by Claim 1. Hence, Huang fails to teach or suggest each state capable of performing a null operation, a write operation, a read operation, and a read/write operation, as recited by Claim 1.

Accordingly, Applicant respectfully submits that the Examiner fails to establish a *prima facie* case of obviousness of Claim 1 over Ledford in view of Huang, since the combination fails to teach or suggest each of the above-recited features of Claim 1. Furthermore, Applicant respectfully submits that establishing a *prima facie* case of obviousness requires a reasonable expectation of success in modifying or combining the reference teachings.

Applicant respectfully submits that the Examiner fails to address the issue of whether the state machine as shown in FIG. 4 of Huang could be incorporated within the state machine 71, as taught by Ledford. Accordingly, Applicant respectfully submits that Claim 1, as amended, is patentable over the combination of Ledford in view of Huang, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 1.

Regarding Claims 7 and 17, Claims 7 and 17 recited the following claim feature, which is neither taught nor suggested by either the combination of Ledford in view of Huang or the references of record:

applying the commands of the test pattern to the test location using a plurality of states, each of the plurality of states being configurable to perform a null operation, a write operation, a read operation, and a read/write operation. (Emphasis added.)

For at least the reasons indicated above with reference to Claim 1, the combination of Ledford in view of Huang fails to teach or suggest a state machine wherein each state is capable

of performing a read operation, a write operation, a read/write operation and a null operation, as recited by Claims 7 and 16. Furthermore, as indicated above, the Examiner fails to illustrate a reasonable expectation of success in modifying state machine 70 of Ledford to incorporate the state machine, as shown in FIG. 4 of Huang.

Therefore, for at least the reasons described above, Applicant respectfully submits that the Examiner fails to establish a *prima facie* case of obviousness of Claims 7 and 16, since the Examiner fails to illustrate a reasonable expectation of success in modifying or combining the references and teachings, and the combination suggested by the Examiner fails to teach or suggest all claim features of Claims 7 and 16.

Accordingly, Claims 7 and 16 are patentable over the combination of Ledford in view of Huang, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 7 and 16.

The Examiner rejects Claims 2, 3, 5, 6, 8-10, 12-14 and 17-19 under 35 U.S.C. §103(a) as being unpatentable over Ledford in view of Huang, as applied to Claim 1, and further in view of U.S. Patent No. 5,825,785 issued to Barry et al. ("Barry"). Applicant respectfully traverses this rejection.

Regarding the Examiner's citing of Barry, Applicant respectfully submits that Claims 1, 7 and 16 are patentable over the combination of Ledford in view of Huang and further in view of Barry, due to the fact that Barry fails to rectify the deficiencies attributed to the combination of Ledford in view of Huang in failing to teach or suggest a plurality of states, each of the plurality of states capable of performing a null operation, a write operation, a read operation and a read/write operation, as recited by Claims 1, 7 and 16. Accordingly, for at least the reasons described above, Applicant respectfully submits that Claims 1, 7 and 16 are patentable over the combination of Ledford in view of Huang and further in view of Barry.

Regarding Claims 2, 3, 5 and 6, Claims 2, 3, 5 and 6 depend from Claim 1 and are therefore patentable over the combination of Ledford in view of Huang and further in view of Barry, based on their dependency from Claim 1. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 2, 3, 5 and 6.

Regarding Claims 8-10 and 12-14, Claims 8-10 and 12-14 depend from Claim 7 and therefore, based on their dependency from Claim 7, are also patentable over the combination of

Ledford in view of Huang and further in view of Barry. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 8-10 and 12–14.

Regarding Claims 17-19, Claims 17-19 depend from Claim 16 and therefore, based on their dependency from Claim 16, are also patentable over the combination of Ledford in view of Huang and further in view of Barry. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.

The Examiner rejects Claims 4, 11 and 20 under 35 U.S.C. §103(a) as being unpatentable over Ledford in view of Huang, as applied to Claims 1, 7 or 16, and further in view of "An Architecture for Synthesis of Testable Finite State Machines" by Agrawal et al. ("Agrawal"). Applicant respectfully traverses this rejection.

Regarding the Examiner's citing of Agrawal, Applicant respectfully submits that the Examiner's citing of Agrawal fails to rectify the deficiencies of the combination of Ledford in view of Huang in failing to teach or suggest a plurality of states, each state capable of performing a null operation, a write operation, a read operation and a read/write operation, as recited by Claims 1, 7 and 16. Accordingly, Claims 1, 7 and 16 are patentable over the combination of Ledford in view of Huang and further in view of Agrawal. Accordingly, Claims 4, 11 and 20, based on their dependency from Claims 1, 7 and 16, respectively, are also patentable over the combination of Ledford in view of Huang and further in view of Agrawal. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 4, 11 and 20.

The Examiner rejects Claim 15 under 35 U.S.C. §103(a) as being unpatentable over Ledford in view of Huang, as applied to Claim 7, and further in view of U.S. Patent No. 6,425,103 issued to Phan ("Phan"). Applicant respectfully traverses this rejection.

Regarding the Examiner's citing of Phan, Applicant respectfully submits that the Examiner's citing of Phan fails to rectify the deficiencies attributed to the combination of Ledford in view of Huang for failing to teach or suggest a plurality of states, each state capable of performing a null operation, a write operation, a read operation and a read/write operation. Accordingly, Claim 15, based on its dependency from Claim 7, is also patentable over the

combination of Ledford in view of Huang and further in view of Phan. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 15.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-20 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: October 26, 2004

By: _____
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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 26, 2004

Marilyn Bass October 26, 2004